Avalanche Hot Source Method for Separated Extraction of Parasitic Source and Drain Resistances in Single Metal-Oxide-Semiconductor Field Effect Transistors

Seok Cheon Baek, Hagyoul Bae, Dae Hwan Kim, and Dong Myong Kim

Abstract—**Separate extraction of source (R_S) and drain (R_D) resistances caused by process, layout variations and long term degradation is very important in modeling and characterization of MOSFETs. In this work, we propose "Avalanche Hot-Source Method (AHSM)" for simple separated extraction of R_S and R_D in a single device. In AHSM, the high field region near the drain works as a new source for abundant carriers governing the current-voltage relationship in the MOSFET at high drain bias. We applied AHSM to n-channel MOSFETs as single-finger type with different channel width/length (W/L) combinations and verified its usefulness in the extraction of R_S and R_D. We also confirmed that there is a negligible drift in the threshold voltage (V_T) and the subthreshold slope (SSW) even after application of the method to devices under practical conditions.**

Index Terms—**MOSFET, source resistance, drain resistance, hot-carrier, parameter extraction, parasitic resistance, avalanche multiplication**

I. INTRODUCTION

Scaling down of MOSFETs (Metal-Oxide-Semiconductor field effect transistors) in CMOS (complementary MOS)-based technology is a primary approach for faster operation and higher integration [1, 2]. Accurate modeling and extraction of characteristic model parameters in MOSFETs, especially parasitic source and drain resistances (R_S and R_D), are crucial to the simulation and implementation of power devices, high performance CMOS devices, and their integrated circuits. With fast scaling down of the device, the total parasitic resistance (R_{SD}=R_S+R_D) is getting comparable to the channel resistance (Rc_h) controlled by the gate voltage [3]. In high frequency and high speed CMOS systems with scaling down of MOSFETs, R_S and R_D play an important role in long term performance degradation and reliability of integrated systems. However, effects of R_S and R_D are different from each other in MOSFETs and integrated circuits [4]. It is well known that the electrical performance and reliability parameters, including transconductance (g_m), saturated drain current ($I_{D,sat}$), cut-off frequency and noise figure, depend more on R_S than on R_D [5, 6]. However, due to the difficulty on the separated extraction of R_S and R_D in MOSFETs without conductive DC gate current through the insulated gate, parasitic resistances are, generally, assumed to be R_S=R_D=R_{SD}/2 regardless of the possible asymmetry in practical MOSFETs. Although several novel methods have been proposed to resolve those issues, those methods are highly complicated or require more than one device or additional patterns for a separated extraction of R_S and R_D [7-15].

In this work, considering asymmetries caused by an intentional and/or accidental layout, process variation, device size and long term degradation, we propose the "Avalanche Hot Source Method (AHSM)" for separated extraction of R_S and R_D in a single MOSFET. In AHSM, the high field region near the drain works as a "hot

Manuscript received Aug. 2, 2011; revised Nov. 21, 2011.
School of Electrical Engineering, Kookmin University, Seoul, Korea
E-mail : dmkim@kookmin.ac.kr

source" for carriers due to the avalanche multiplication process and the current-voltage relationship is limited by the R_D at high drain bias [16, 17]. We applied the proposed method to n-channel MOSFETs with different channel width/length (W/L) combinations and verified its usefulness in robust extraction of R_S and R_D.

II. AVALANCHE HOT SOURCE METHOD FOR SEPARATED EXTRACTION OF RS AND RD IN MOSFETS

Carriers flowing in n-channel MOSFETs under avalanche multiplication at large drain bias (V_{DS}) are schematically shown in Fig. 1 including R_S (source resistance), R_D(drain resistance), R_G (gate resistance) and R_B (substrate resistance). The component ① describes channel electrons moving from the source to the drain in n-channel MOSFETs at the gate voltage (V_{GS}) greater than the threshold voltage (V_T). Components ②~⑤ are for electron-hole pairs (EHPs) generated by the impact ionization of hot carriers in the high field region near the drain at a large V_{DS}. Component ② is for lucky hot electrons injected into the gate oxide by the vertical field and ③ for electrons drifted to the drain by the lateral field after impact ionization. Components ④ and ⑤ are for moving holes after EHP generation by impact ionization due to hot electrons in the channel. The component ③ is for electrons collected to the drain in the high field region close to the drain. In AHSM for separated extraction of R_S and R_D in MOSFETs, we focus on the current component ③ at large drain bias in MOSFETs for characterization [18, 19].

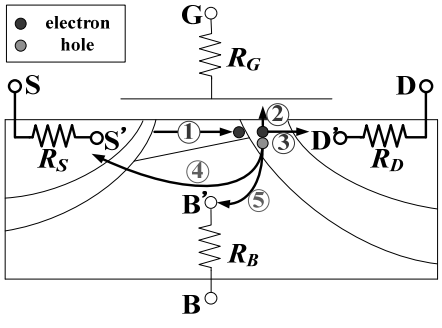

Fig. 1. Schematic illustration of carriers moving in n-channel MOSFET under large drain bias (V_{DS}) with parasitic source (R_S), drain (R_D), gate (R_G) and substrate (R_B) resistances. The component ③ is for electrons collected to the drain in the high field region close to the drain and this is a main component for AHSM in the separated extraction of R_S and R_D in MOSFETs.

Meanwhile, in the saturation mode of MOSFETs under a large V_{DS} ($V_{Dsat}<V_{DS}<V_{Do}$) without avalanche multiplication by hot channel carriers, the normal saturated drain current ($I_{D,sat}$) with a channel length modulation (λ) is described by

$$I_{D,sat} \cong \begin{cases} \dfrac{\mu_{eff} C_{ox}}{2}\left(\dfrac{W}{L}\right)\left(V_{GS}-V_T-I_{D,sat}R_S\right)^2\left[1+\lambda\left\{V_{DS}-I_{D,sat}\left(R_S+R_D\right)\right\}\right] \\ : pinch-off \\ C_{ox}W\left(V_{GS}-V_T-V_{Dsat}-I_{D,sat}R_S\right)\upsilon_{sat} \\ : velocity\ saturation \end{cases} \quad (1)$$

with μ_{eff}=the effect channel carrier mobility, C_{ox}=the oxide capacitance per unit area, λ=the channel length modulation parameter, υ_{sat}=the saturation velocity of the channel carriers in short channel MOSFETs and V_{Dsat}=the drain saturation voltage ($V_{Dsat}=V_{GS}-V_T$ in long channel and $V_{Dsat}\approx L\varepsilon_{sat}$ in short channel MOSFETs. : ε_{sat} is the saturation field in the channel). The gate bias-dependent critical drain voltage V_{Do} is defined as the drain voltage at the turn-on of the avalanche multiplication process in MOSFETs. If the drain current is sharply increased by the component ③ due to EHPs generated by hot channel carriers at $V_{DS}>V_{Do}$, the internal drain voltage V_{DS0} is not controlled by V_{GS} or V_{DS} as in MOSFETs. The internal drain voltage is defined to be $V_{DS0}=V_{DS}-I_D(R_S+R_D)$ as the real drain-to-source voltage after de-embedding the voltage drop across parasitic R_S and R_D. Although the amount of EHP is determined by the inversion charges through the vertical field by V_{GS} and the lateral field by V_{DS}, the variation in V_{D0} is negligible.

Fig. 2 shows the field distribution under a specific bias, the relative amount of EHP and location of effective hot source with this distribution. Fig. 2 clearly tell that the source of the current generated by the component ③ ends up to be close to the drain edge regardless of ΔL ($\Delta L = L-L_{eff}$(L=gate length, L_{eff}=effective channel length)). Therefore, the internal drain voltage and the amount of EHP are limited by the voltage drop across R_D. This is because most of the avalanche-generated excess electrons are collected to the drain and causes a voltage drop only across R_D. In this case, the drain current I_D and I_{Do} after the turn-on of the avalanche multiplication ($V_{DS}>V_{Do}$) is

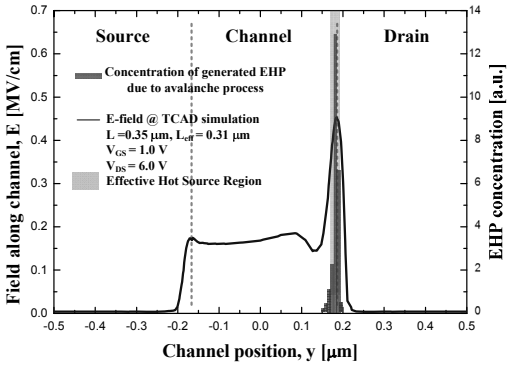

Fig. 2. General E-field distribution of certain device (W=120 μm, L=0.35 μm, L_{eff}=0.31 μm, V_{GS}=1.0 V, V_T = 650 mV and V_{DS}=6.0 V) and EHP concentration generated spatially and location of effective hot source from Avalanche Hot source region with similar general E-field distribution.

described by the sum of two current components (I_{Do} and $I_{D,hot}$; component ③), as schematically shown in Fig. 3(b) as an inset,

$$I_D = I_{Do} + I_{D,hot} \tag{2}$$

$$I_{Do} \equiv I_D\big|_{V_{DS}=V_{Do}} \text{ in Eq. (1)} \tag{3}$$

$$I_{D,hot} = qn_{ch}(1+M)\upsilon_{sat}W = \frac{(V_{DS}-V_{Do})}{R_D} \text{ with avalanche process at } V_{DS} > V_{Do}. \tag{4}$$

Therefore, we finally obtain

$$I_D = I_{Do} + I_{D,hot} = I_{Do} + \frac{V_{DS}-V_{Do}}{R_D} (\text{for } V_{DS} > V_{Do}) \tag{5}$$

for the AHSM under large drain bias with I_{Do}=the normal drain current at V_{DS}=V_{Do} without the avalanche process, M=the avalanche multiplication factor and n_{ch}=V_{GS}-controlled channel carrier concentration.

$I_{D,hot}$ is defined as the hot-carrier-induced avalanche drain current after the turn-on of the avalanche multiplication process by the impact ionization of hot channel carriers. Due to an abrupt increase of the hot channel carriers, the drain region with the high electric field works as a hot source and the current is limited by the extrinsic drain resistance R_D.

Although the absolute value of the drain current I_D=I_{DO}+$I_{D,hot}$ depends on the bias condition and the device structure, the slope ($\partial I_D/\partial V_{DS}$) is prominently determined by R_D because the avalanche-generated carrier-limited drain current $I_{D,hot}$=(V_{DS}-V_{Do})/R_D in the hot source region under large bias V_{DS}>V_{Do}. Therefore, it is possible to extract R_D from the slope of the I_D-V_{DS} characteristics with a controlled avalanche process at V_{DS}>V_{Do} using

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{R_D} (\text{for } V_{DS} > V_{Do}) \tag{6}$$

This is the "Avalanche Hot Source Method" for separated extraction of R_D from R_S in R_{SD} because the high field region near the drain works as a new carrier source/supplier (*avalanche hot source*) of a large amount of excess EHP's governing the current-voltage relation in the MOSFET with parasitic resistances under the high field formed by the large drain bias.

III. EXPERIMENTAL RESULTS : SEPARATED EXTRACTION OF RD AND RS

Experimental I_D-V_{DS} characteristics of the n-channel MOSFET (thickness of the gate oxide: t_{ox}=7.3 nm, gate width/length W/L=120 μm/0.35 μm and typical overlap length = 0.045 μm fabricated using a 0.35 μm CMOS process) are shown in Fig. 3. The threshold voltage and the subthreshold slope were measured to be V_T=662~668 mV and SSW=81~83.5 mV/dec, respectively, from MOSFETs with various W/L-combinations as summarized in Table I. In the I_D-V_{DS} characteristics for MOSFETs under test, there are four different regions to be categorized: a) Linear region with V_{DS}<V_{Dsat}, b) Saturation region with V_{Dsat}<V_{DS}<<V_{Do}, c) Transition region for V_{Dsat}<<V_{DS}<V_{Do} with an increasing I_D and d) Avalanche hot source region with a constant slope in the I_D-V_{DS} characteristics at V_{DS}>V_{Do}.

In the hot source region under high drain bias (V_{Do}>5.0~5.7 V for V_{GS}=1.0~1.4 V), the slope in the I_D-V_{DS} curve is constant and R_D is obtained from 1/slope as shown in Fig. 3(b). As expected, the hot source turn-on voltage V_{Do} depends on V_{GS} because the carrier density available to the avalanche process for the hot source is increasing with V_{GS}.

Even at a low gate voltage (V_{GS}>V_T), the AHSM gives a relatively accurate R_D. This is because the effective hot source region moves far from the drain with increased charges supplied from the channel, as shown in Fig. 2.

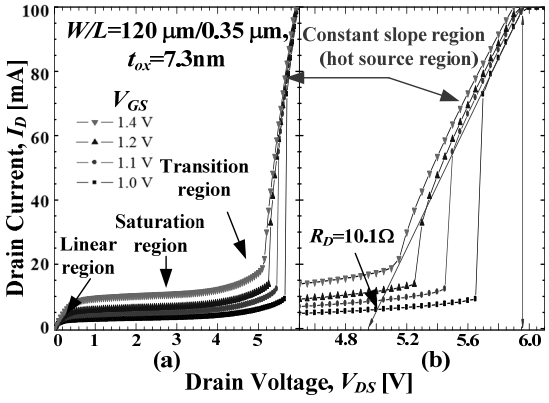

Fig. 3. I_D-V_{DS} characteristics of n-channel MOSFET (t_{ox}=7.3 nm and W/L=120 μm/0.35 μm). (a) Over a wide range of the drain bias V_{DS} (b) The hot source region with avalanche multiplication at large drain bias for AHSM. In the constant slope region, 1/slope=R_D is independent of the gate bias. The equivalent circuit for the MOSFET with the avalanche hot carrier multiplication is schematically shown in Fig. 1.

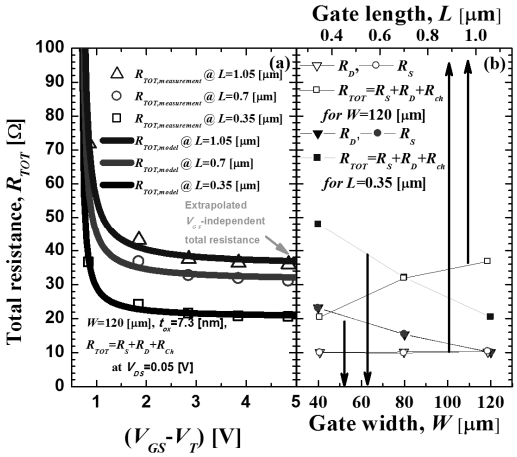

Fig. 4. Resistances obtained from experimental I_D-V_{DS} characteristics in linear region (V_{DS}=0.05V) of n-channel MOSFETs. (a) V_{GS}-dependent total resistance R_{TOT}=R_S+R_D+R_{Ch} for MOSFET with W=120 μm and L=0.35, 0.7, 1.05 μm. (b) R_S and R_D obtained from AHSM applied to MOSFETs with various W/L combinations.

The gate-bias dependent total resistance R_{TOT} (R_{TOT}= R_S+R_D+R_{Ch} with R_{Ch}=channel resistance) obtained from I_D-V_{DS} characteristics in the linear region with a small V_{DS} (=0.05 V) is shown in Fig. 4(a) for n-channel MOSFETs with W=120 μm and L=0.35, 0.70 and 1.05 μm. Therefore, the total source-to-drain resistance R_{TOT} can be obtained from

$$R_{TOT}(V_{GS}) \equiv \frac{V_{DS}}{I_D} = R_{SD} + \frac{L_{eff}}{\mu_{eff} C_{ox} W (V_{GS} - V_T)} = R_{SD} + R_{Ch} = R_{SD} + L_{eff} \times r_{ch} \quad (7)$$

with V_{GS}-independent R_{SD}≡R_S+R_D, including a V_{GS}-dependent channel resistance and channel resistance per unit channel length (r_{ch}) [20].

R_S and R_D extracted by the proposed AHSM are shown in Fig. 4(b) for different W/L combinations (W/L=40/0.35, 80/0.75, 120/0.35, 120/0.7, 120/1.05 μm/μm) of n-channel MOSFETs. The channel resistance R_{Ch} strongly depends on the gate bias for the MOSFET under characterization. As far as we obtain R_S and R_D from AHSM, R_{Ch} can be obtained from R_{Ch}=R_{TOT}-(R_S+R_D) from the extracted R_{TOT} in the I_D-V_{DS} characteristics under the linear mode of operation with a small V_{DS}. R_S and R_D obtained by AHSM are extracted to be R_S=10.1~23.2 Ω and R_D=9.9~23.1 Ω for MOSFETs as summarized in Table I for different W/L combinations on the same wafer. We also summarized the normalized value of the resistance as (R×W~12 MΩ·cm) for verification of the gate width effect.

In the Table 1, the R×W for W=40 μm is small because the effective channel width (W_{eff}) becomes wider with decreasing the gate width. It clearly shows that the AHSM reflects a change depending on the device size. We also note that there is a shift in the ratio of R_{SD} to R_{TOT} when the gate length changes [3] because the channel resistance (R_{Ch}) depends on both the gate bias and channel length while R_S and R_D are independent of of them. Lastly, we also checked the change of device parameters after 20 times of repeated hot-source

Table 1. Extracted R_S and R_D by Avalanche Hot Source Method (AHSM)

***W/L* [μm/ μm]**	**40/0.35**	**80/0.35**	**120/0.35**	**120/0.7**	**120/1.05**
V_T [mV]	668	663	662	664	663
ΔV_T[mV]	10	31	57	40	31
SSW [mV/dec]	83.5	81	81.4	83.3	82.7
ΔSSW [mV/dec]	4.8	3.9	3.9	2.4	1.3
R_{TOT}[Ω] @V_{GS}=5.5,V_{DS}=0.05V	47.92	32.03	20.45	31.88	36.79
ΔR_{TOT}[Ω]	13.66	6.02	0.64	1.71	3.55
R_S[Ω]	23.2	15.3	10.1	10.2	10.2
R_D[Ω]	23.1	15.4	10.0	9.9	10.4
ΔR_S[Ω]	<±1%	<±1%	<±1%	<±1%	<±1%
ΔR_D[Ω]	<±1%	<±1%	<±1%	<±1%	<±1%
(R_D+R_S)/ R_{TOT} @V_{GS}=5.5,V_{DS}=0.05V	96.6%	95.8%	98.3%	63.0%	56.0%
R·W [MΩ·cm]	9.3	12.3	12.1	12.1	12.4

characterization for each device and the result is summarized in Table I. Small changes in V_T and *SSW* are expected due to the hot carrier stress during the hot source characterization with the avalanche multiplication process for $V_{DS}>V_{Do}$, but we observed no considerable drift in the parameters. This is because AHSM can be performed only once or twice in order to extract R_D.

These results show that separated R_S and R_D are extracted consistently by the AHSM without causing any significant device performance degradation during characterization.

IV. CONCLUSIONS

We proposed a new technique for separated extraction of R_S (source resistance) and R_D (drain resistance) in MOSFETs considering possible asymmetries in layout, process variation and long term degradation of MOSFETs. It was named as "Avalanche Hot Source Method" because the high field region near the drain at a high drain voltage (V_{DS}) works as a new carrier source of excess EHP's and the extra drain current $I_{D,hot}$ due to avalanche multiplication governing the current-voltage relation in MOSFETs with parasitic R_S and R_D. Under avalanche multiplication, the drain current is limited by R_D in MOSFETs and we obtained R_D from the slope of I_D-V_{DS} curves in the avalanche hot carrier-dominant operation region at a high V_{DS}. We applied the AHSM to n-channel MOSFETs with several *W/L* combinations and verified its usefulness in the extraction of separated R_S from R_D. We also confirmed that there was no considerable drift in V_T and *SSW* even after application of the method to MOSFETs under test with practical conditions.

ACKNOWLEDGMENTS

This work was supported by the National Research Foundation (NRF) of Korea grant funded by the Korean Government (MEST) (Grant No.2009-0071088) and in part by the Kookmin University Research Initiative Program(2011). The CAD software was supported by SILVACO and IDEC.

REFERENCES

[1] S. C. Williams, et al, "Scaling Trends for Device Performance and Reliability in Channel Engineered n-MOSFET's," *IEEE Trans. Electron Devices*, Vol.45, No.1, pp.254-260, Jan., 1998.

[2] H. Iwai, H. S. Momose and Y. Katsumata, "Si-MOSFET scaling down to deep-sub-0.1-micron range and future of silicon LSI," *VLSI Technology (Systems and Applications International Symposium)*, pp.262-267, 1995.

[3] N. Arora, *MOSFET Models for VLSI Circuit Simulation*, World scientific, 1993, pp.102-108.

[4] S. Cserveny, "Relationship between measured and intrinsic transconductances of MOSFET's," *IEEE Trans. Electron Devices,* Vol.37, No.11, pp.2413-2414, Nov., 1990.

[5] J. F. Chen, J. Tao, P. Fang, and C. Hu, "0.35 μm asymmetric and symmetric LDD device comparison using a reliability/speed/power methodology," *IEEE Electron Dev. Lett.*, Vol.19, No.7, pp.216-218. Jul., 1998.

[6] J. F. Chen, J. Tao, P. Fang, and C. Hu, "Performance and reliability comparison between asymmetric and symmetric LDD devices and logic gates," *IEEE Solid-State Circuits*, Vol.34, No.3, pp.367-371, Mar., 1999.

[7] C. L. Lou, W. K. Chim, D. D. S. Chan, and Y. Pan, "A novel single device DC method for extraction of the effective mobility and source-drain resistance of fresh and hot-carrier degraded drain-engineered MOSFET's," *IEEE Trans. Electron Devices*, Vol.45, No.6, pp.1317-1323, Jun., 1998.

[8] H. T. Kim, I. C. Nam, K. S. Kim, K. H. Kim, J. B. Choi, J. U. Lee, S. W. Kim, G. C. Kang, D. J. Kim, K. S. Min, D. W. Kang, and D. M. Kim, "Extraction of the Source and Drain Resistances in MOSFETs using Parasitic Bipolar Junction Transistor," *Electronics Lett*., Vol.41, No.13, pp.772-774, Jun., 2005.

[9] D. M. Kim, H. C. Kim, and H. T. Kim, "Modeling and Extraction of Gate Bias-Dependent Parasitic Source and Drain Resistances in MOSFET's," *Solid-State Electronics*, Vol.47, No.10, pp.1707-1712, Oct., 2003.

[10] E. Torres-Rios, R. Torres-Torres, G. Valdovinos-Fierro, and E. A.Gutiérrez-D, "A method to determine the gate bias-dependent and gate bias-independent components of MOSFET series resistance from S-parameters," *IEEE Trans. Electron*

Devices, Vol.53, No.3, pp.571-573, Mar., 2006.

[11] J. C. Guo, S. S. Chung, and C. C. H. Hsu, "A new approach to determine the effective channel length and drain-and source series resistance of miniaturized MOSFET's," *IEEE Trans. Electron Devices*, Vol.41, No.10, pp.1811-1818, Oct., 1994.

[12] A. Ortiz-Conde, J. J. Liou, W. Wong, and F. J. Garcia Sanchez, "Simple method for extracting the difference between the drain and source series resistances in MOSFETs," *Electron Lett*, Vol.30, No.12, pp.1013-1015, Jun., 1994.

[13] A. Raychaudhuri, J. Kolk, M. J. Deen, and M. I. H. King, "A simple method to extract the asymmetry in parasitic source and drain resistances from measurements on a MOS transistor," *IEEE Trans. Electron Devices*, Vol.42, No.7, pp.1388-1390, Jul., 1995.

[14] S. H. Jen, C. C. Enz, D. R. Pehlke, M. Schroter, and B. J. Sheu, "Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz," *IEEE Trans. Electron Devices*, Vol.46, No.11, pp.2217-2227, Nov., 1999.

[15] S. Lee, H. K. Yu, C. S. Kim, J. G. Koo, and K. S. Nam, "A novel approach to extract small-signal model parameters of silicon MOSFET's," *IEEE Microwave Guided Wave Lett.* Vol.7, No.3, pp.75-77, Mar., 1997.

[16] A. T. Hatzopoulos, D. H. Tassis, and C. A. Dimitriadis, and G. Kamarinos, A. T. Hatzopoulos, D. H. Tassis, and C. A. Dimitriadis, and G. Kamarinos, "Analytical on-state current model of polycrystalline silicon thin-film transistors including the kink effect," *Appl. Phys. Lett.,* Vol.87, No.6, p.063501, Aug., 2005.

[17] E.-H. Toh, G. H. Wang, L. Chan, G. Samudra, and Y.-C. Yeo, "Reduction of impact-ionization threshold energies for performance enhancement of complementary impact-ionization metal-oxide-semiconductor transistors," *Appl. Phys. Lett.,* Vol.91, No.15, p. 153501, Oct., 2007.

[18] R. S. Muller, T. I. Kamins, and M. Chan, *Device Electronics for Integrate Circuits*, John Wiley & Sons, 2003, pp.490-507.

[19] Y. Taur, T. Ning, *Fundamentals of MODERN VLSI DEVICES*, Cambridge university press, 1998, pp.158-161.

[20] H. Bae, S. C. Baek, S. Lee, J. Jang, J. S. Shin, D. Yun, H. Kim, D. H. Kim, and D. M. Kim, "Separate Extraction of Source, Drain, and Substrate Resistances in MOSFETs With Parasitic Junction Current Method," *IEEE Electron Device Lett.*, Vol.31, No.11, pp.1190-1192, Nov., 2010.

Seok Cheon Baek received the B.S. degree in electronics engineering from Kookmin University, Seoul, Korea, in 2008, where he is currently working toward Samsung Electronics Company, Ltd., Kyung ki-Do, Korea. His research interests include characterization and modeling of silicon nanostructure devices, and their device physics.

Hagyoul Bae received the B.S. and M.S. degrees in electronics engineering from Kookmin University, Seoul, Korea, in 2007 and 2010, respectively. His current research interests include characterization and modeling of silicon nanostructure devices, amorphous oxide semiconductor thin film transistors (TFT), flash memory devices, and their device physics.

Dae Hwan Kim received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2002, respectively. From 2002 to 2005, he was with Samsung Electronics Company, Ltd., Kyung ki-Do, Korea, where he contributed to the design and development of 92-nm double data rate (DDR) dynamic RAM (DRAM) and 80-nm DDR2 DRAM. In 2005, he joined the School of Electrical Engineering, Kookmin University, Seoul, where he is currently an Associate Professor. He has authored or coauthored more than 170 research publications and patents. His current research interests are nanoscale CMOS devices and integrated circuits, metal oxide and organic thin-film transistors, biosensors devices, exploratory logic and memory devices, energy-efficient nano-ICs, and Si quantum devices. He has also worked on the characterization, modeling, and circuit design for reliabilities of CMOS devices, thin-film transistors, display, biosensors, and neuromorphic systems.

Dr. Kim is a member of the IEEE Electron Devices Society, the Society for Information Display, the Electrochemical Society and the Institute of Electronics Engineers of Korea.

Dong Myong Kim received the B.S. (magna cum laude) and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1986 and 1988, respectively, and the Ph.D. degree in electrical engineering from the University of Minnesota, Twin Cities, in 1993. From February 1988 to August 1989, he was with the Division of Electronic Engineering at Korea Institute of Science and Technology (KIST), Seoul, Korea, where he worked on the characterization and modeling of microwave devices and integrated circuits. Since March 1993, he has been with the School of Electrical Engineering, Kookmin University, Seoul, Korea. He is also serving as a Special Lecturer for Semiconductor Physics and Devices at Samsung Electronics Co., Hwasung, Korea since April 2002. His current research interests include design, fabrication, characterization, and modeling of nanostructure silicon devices, thin film transistors, biosensors, III–V compound semiconductor devices, volatile and nonvolatile memories, and CMOS RF circuits.