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Semicond. Sci. Technol. **25** (2010) 035004 (6pp) doi:10.1088/0268-1242/25/3/035004

Structural optimization of extremely scaled planar partially insulated field effect transistors (PiFETs)

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Received 2 February 2009, in final form 3 December 2009
Published 29 January 2010
Online at stacks.iop.org/SST/25/035004

Abstract

The effects of both the separation between two partially insulated oxide layers (L_{PiOX}) and the thickness of a partially insulated oxide layer (T_{PiOX}) on the short channel effect (SCE) and the intrinsic propagation delay in partially insulated field-effect transistors (PiFETs) are investigated by using technology computer-aided design (TCAD) device simulation. The reverse SCE can be suppressed by controlling the tilt angle of halo implantation to $T_{\mathrm{tilt}} = 55^{\circ}$. In the case of a PiFET with the channel length (L_g), as L_{PiOX}/L_g decreases, the subthreshold swing becomes smaller while the drain-induced barrier lowering does larger. The L_{PiOX}/L_g and T_{PiOX} dependence of the intrinsic propagation delay results from the variation of the junction capacitance (C_j). C_j is more sensitive to T_{PiOX} rather than L_{PiOX}/L_g. Conclusive optimal conditions for both SCE and the intrinsic propagation delay are summarized as $L_{\mathrm{PiOX}}/L_g = 0.6$–$0.65$, $T_{\mathrm{PiOX}} \geqslant 60$ nm and $T_{\mathrm{tilt}} = 55^{\circ}$, respectively.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

As the scaling of the conventional CMOS technology proceeds, the improvement of both the performance and the power consumption becomes inevitably more difficult and the short channel effects (SCEs) also become more challenging to control on the platform of the bulk silicon. Because of the better immunity to SCEs and high performance, SOI (silicon-on-insulator) technology has been considered as one of promising candidates for meeting these requirements [1, 2]. In spite of many advantages of the self-limited shallow junction, simple and compatible process with planar CMOS technology, low power consumption and higher switching speed, technological hurdles including the threshold voltage (V_T) controllability, floating body effect, self-heating, the history effect in logic operations and back gate interface problem must be overcome. To surmount these hurdles, PiFETs (partially-insulated field-effect transistors) have been proposed as a useful approach to a nano-scale hybrid SOI/bulk CMOS technology pursuing both the high performance and the low power consumption [3], and their applications such as DRAM cell transistor [4–6] have been successfully demonstrated based on novel controllable process technologies with a selective etch of SiGe [3], local damascene [6, 7] and/or pad-polysilicon side contacts (PSC) [5]. The PiOX (partially insulated oxide) layer located just beneath the source/drain (S/D) region suppresses the junction capacitance, and acts as a diffusion barrier resulting in self-induced halo regions near its edge. In addition, the moderate threshold voltage (V_T) is possible and the thermal instability by the self-heating effects is suppressed due to the thermal conduction through the space between two PiOX layers. This phenomenon contributes to reducing both SCEs and the junction leakage current [8]. On the other hand, although both the immunity to SCEs and the circuit performance depend strongly on the parameters such as the separation between two PiOX layers (L_{PiOX}) and the thickness of PiOX layers (T_{PiOX}), the structural optimization in PiFETs has been rarely studied.

In this work, the structural optimization in PiFETs is performed as a design guide by investigating the dependence of both SCE and the intrinsic delay on L_{PiOX} and T_{PiOX} through the technology computer-aided design (TCAD) device simulation.

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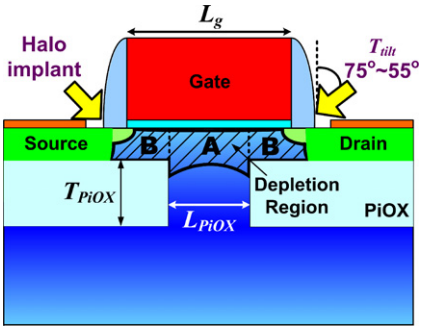

Figure 1. Schematic cross-sectional view of PiFETs.

In detail, the V_T roll-off, the saturation current (I_{DSAT}), the subthreshold swing (SSW), drain-induced barrier lowering (DIBL), total gate capacitance (C_{total}), the source/drain junction capacitance (C_j) and the intrinsic propagation delay (τ) are investigated as L_{PiOX}- and T_{PiOX}-dependent figures of merits.

2. Device simulation platform

A schematic cross-sectional view of PiFETs used in the device simulation is shown in figure 1. The process/device simulation is performed by the ISE TCAD tool (SENTAURUS PROCESS and DEVICE 2D simulator) [9, 10]. We used the Sentaurus-Mesh for mesh generation in the TCAD simulation, and the number of total mesh was 9000 nodes (vertexes). For the simulation time and accuracy, in mesh strategy, we built dense meshes both in the abrupt junction and channel areas. On the other hand, meshes of other region are coarse in the Sentaurus process and device simulation. A hydrodynamic (energy balance) transport model is used in the simulation to provide a physically accurate result. Transient behavior was also simulated for ac simulation. A mobility model with the doping dependence, high-field saturation (velocity saturation) and transverse field dependence is used for this simulation. The SRH recombination and the band to band tunneling models are used in the regions close to insulator interfaces and rapid changing electric field regions.

We added simulation detail in the revised manuscript.

Initial p-type doping concentration in Si substrate (N_A) is 1×10^{15} cm^{-3}, and the work function of n$^+$-doped poly-Si gate is 4.01 V. The top Si layer thickness (T_{Si}) is 12 nm, and the equivalent oxide thickness (EOT) is 0.8 nm (EOT of extended planar bulk MOSFETs in International Technology Roadmaps for Semiconductors (ITRS) 2009–2010) [11]. In order to circumvent the overestimation of the L_{PiOX} and T_{PiOX} dependence of PiFET device characteristics, a thin EOT is employed. Because L_{PiOX} and T_{PiOX} play more significant roles on C_j rather than the intrinsic gate capacitance C_g, the ratio C_j/C_{total} is intentionally shrunk by increasing C_g/C_{total} through an ultra-thin EOT. Most device process sequence is described in [3]. V_T is adjusted to 0.2 V by implanting indium ions (In, 8×10^{14} cm^{-2}, 70 keV with a sacrificial oxide layer) to form a super-steep retrograde (SSR) channel doping profile [12]. After the gate patterning, n$^+$ S/D extension regions are formed by As ion implantation with 4×10^{13} cm^{-2}, 20 keV. Then, the formation of the spacer is followed by the halo implantation with In ion (4×10^{13} cm^{-2}, 35 keV, and the tilt angle of T_{tilt}). Deep S/D regions are formed by As ion implantation with 5×10^{15} cm^{-2}, 20 keV, and the rapid thermal anneal is followed by activate dopants at 1050 °C for 10 s. The final channel doping concentration at the surface is 5×10^{18} cm^{-3}. Although the formation of the self-induced halo region in PiFETs effectively suppresses DIBL [8], an additional halo implantation is performed in this case to control the reverse SCE (RSCE) as described later. Furthermore, the dose of halo implantation is chosen to be moderate in order to control the junction leakage current.

3. Short channel effects in PiFETs

Compared with conventional MOSFETs, the V_T roll-off with decreased channel length (L_g) due to the shared depletion charges between S/D and the channel region becomes more complicated in PiFETs. Actually, the RSCE of PiFETs has been observed in previously reported experimental data. It is attributed to the competition between the self-induced halo doping charge volume and the depletion charge volume shared by S/D and the channel region. Therefore, the RSCE would be strongly correlated with the angle of halo implantation (T_{tilt}). On the other hand, in the viewpoint of the self-induced halo doping in a PiFET [7, 8, 13], the lateral location of the peak in the halo doping concentration (along the channel length direction) is varied with both L_g and L_{PiOX} because the eventual halo doping concentration after the dopant activation sequence is dependent on L_{PiOX}/L_g while the lateral location of the As-implanted halo doing region is determined only by L_g. This condition agrees with the actual process sequence [3, 4]. As L_{PiOX}/L_g decreases, the highly doped region by halo implantation is more locally agglomerated due to the diffusion-barrier role of the PiOX layer. In our case, the RSCE is investigated under the condition of $L_{PiOX}/L_g = 1$ assuming that the condition of $L_{PiOX}/L_g = 1$ is the worst case. This is reasonable because the self-induced halo doping in a PiFET is still effective for $L_{PiOX}/L_g \leqslant 1$. Figure 2 shows the T_{tilt} dependence of V_T roll-off characteristics. This results show that the RSCE can be suppressed by controlling T_{tilt} and the optimal condition is $T_{tilt} = 55°$.

Figure 3 shows the L_{PiOX} and T_{PiOX} dependences of both SSW and DIBL. As L_{PiOX}/L_g decreases, SSW becomes smaller while DIBL becomes larger. The top Si layer is so thin like an ultra-thin-body (UTB) MOSFET (=12 nm) that the vertical position of the boundary between the depletion region and the neutral region is located between two PiOX layers as shown in figure 1.

We note that the depletion charge on the PiOX layer Q_{dB} (B region in figure 1) makes a negligible influence on SSW due to the thick buried oxide. Therefore, the depletion charge Q_{dA} (related to the depletion capacitance) in the A-region in figure 1 plays a major role in SSW. Consequently, as L_{PiOX}/L_g decreases, the reduction of Q_{dA} results in more improved subthreshold slope. On the other hand, as L_{PiOX}/L_g decreases, DIBL becomes larger because the high doping region of V_T

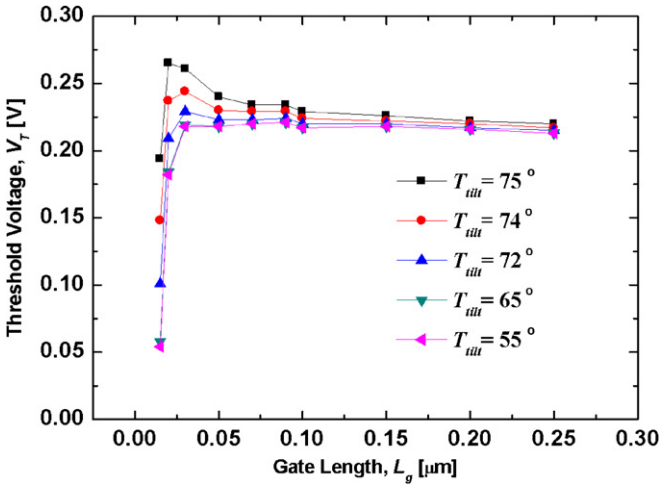

Figure 2. V_T roll-off characteristic of PiFETs and the T_{tilt} dependence of the RSCE.

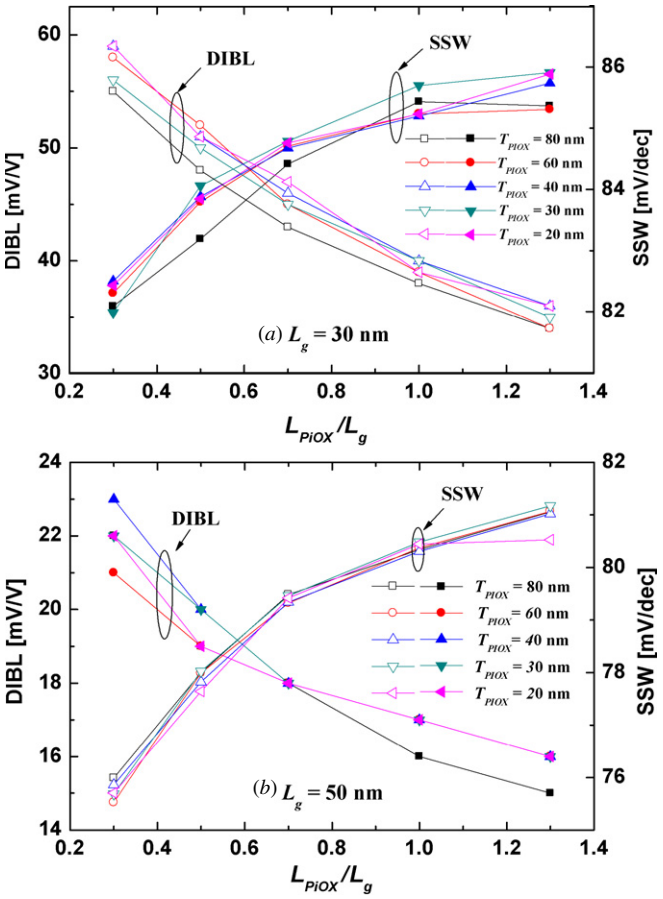

Figure 3. L_{PiOX} and T_{PiOX} dependences of both SSW and DIBL. (*a*) $L_g = 30$ nm (*b*) $L_g = 50$ nm.

adjustment implantation becomes located farther from S/D edge as shown in figure 4. In other words, two PiOX layers play as diffusion barriers when the high doping region of SSR implantation laterally diffuses. In addition, both *DIBL* and *SSW* are independent of T_{PiOX} as shown in figure 3. From this result, the optimal condition with respect to the SCE is observed to be $L_{\text{PiOX}}/L_g = 0.6$–$0.65$.

Table 1. The comparison of SCEs between SOI MOSFETs and PiFETs.

L_g	Parameter	SOI MOSFETs	PiFETs
50 nm	V_T (V)	0.11	0.2
	SSW (mV dec^{-1})	68.6	78.8
	DIBL (mV V^{-1})	31.4	21.5
30 nm	V_T (V)	0.08	0.21
	SSW (mV dec^{-1})	79.3	89.3
	DIBL (mV V^{-1})	83.8	54.2

I_{DS}-V_G characteristics of PiFETs ($L_{\text{PiOX}}/L_g = 0.65$) compared with those of SOI MOSFETs (the thickness of buried oxide layer = 80 nm) are shown in figure 5. The key parameters are summarized in table 1. V_T is measured by the definition as the gate voltage (V_g) at which the drain current (I_{DS}) at the supply voltage (V_{DD}) = 1.1 V has the value of 0.1 μA μm^{-1}. Although SSW of PiFETs is slightly higher than those of SOI MOSFETs, both SSW and DIBL of optimized PiFETs show a better SCE immunity in comparison with the experimental data [8]. In addition, it is worth to note that the RSCE is effectively suppressed even for $L_{\text{PiOX}}/L_g = 0.65$ as summarized in table 1.

4. Intrinsic propagation delay and junction load capacitance in PiFETs

In order to investigate the L_{PiOX} and T_{PiOX} dependence of the circuit performance as well as the SCE immunity, the intrinsic propagation delay (τ) should be estimated with I_{DSAT}, C_{total} and V_{DD} as described by

$$\tau = \frac{C_{\text{total}} V_{\text{DD}}}{I_{\text{DSAT}}}. \quad (1)$$

Figure 6 shows the V_{DD} dependence of I_{DSAT} as a function of T_{PiOX} and L_g. While I_{DSAT} is a strong function of both V_{DD} and L_g, it is insensitive to T_{PiOX}. It means that the influence of fringing field effect through the PiOX layer on dc characteristics is not significant. The L_{PiOX} dependence of I_{DSAT} is due to the gate controllability through the depletion charge Q_d. The increase of Q_d resulting from the increased L_{PiOX} with a fixed L_g is followed by both the increased V_T and the decreased I_{DSAT}.

The C_{total}–V_g curves as the functions of L_g, L_{PiOX}/L_g and T_{PiOX} are shown in figure 7. While C_{total} is insensitive to T_{PiOX}, the L_{PiOX}/L_g dependence of C_{total} is clearly observed especially in a weak inversion region. Because L_{PiOX} and T_{PiOX} play more significant roles of C_j rather than C_g, the L_{PiOX}/L_g dependence of C_{total} is originated from that of C_j. Therefore, the L_{PiOX}/L_g dependence of τ results from the effect of C_j component.

Under a fixed L_g, in order to improve τ, C_j should be shrunk by optimizing L_{PiOX}/L_g and T_{PiOX}. Figure 8 shows the C_j–V_g curves extracted from the TCAD simulation (INSPECTOR) as the functions of L_g, L_{PiOX}/L_g and T_{PiOX}. Our results show that C_j is more sensitive to T_{PiOX} than L_{PiOX}/L_g. Trying to reduce C_j by the extremely small L_{PiOX}/L_g would be very ineffective because that the PiFET becomes more susceptible to self-heating as observed in SOI MOSFETs while

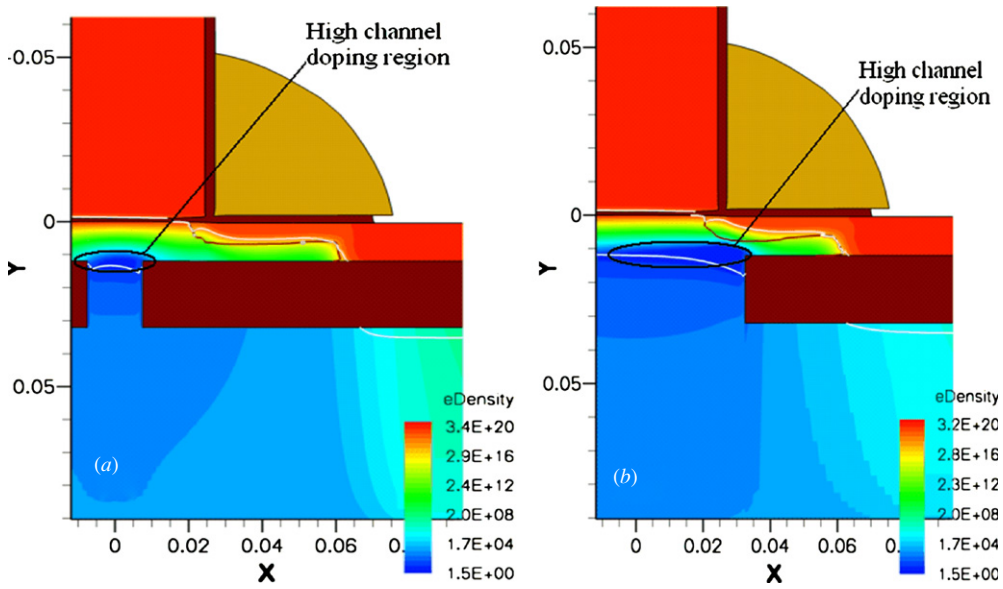

Figure 4. The electron density from the channel center to the drain edge of PiFETs with $L_g = 50$ nm. (*a*) $L_{\mathrm{PiOX}}/L_g = 0.3$ and (*b*) $L_{\mathrm{PiOX}}/L_g = 1.3$.

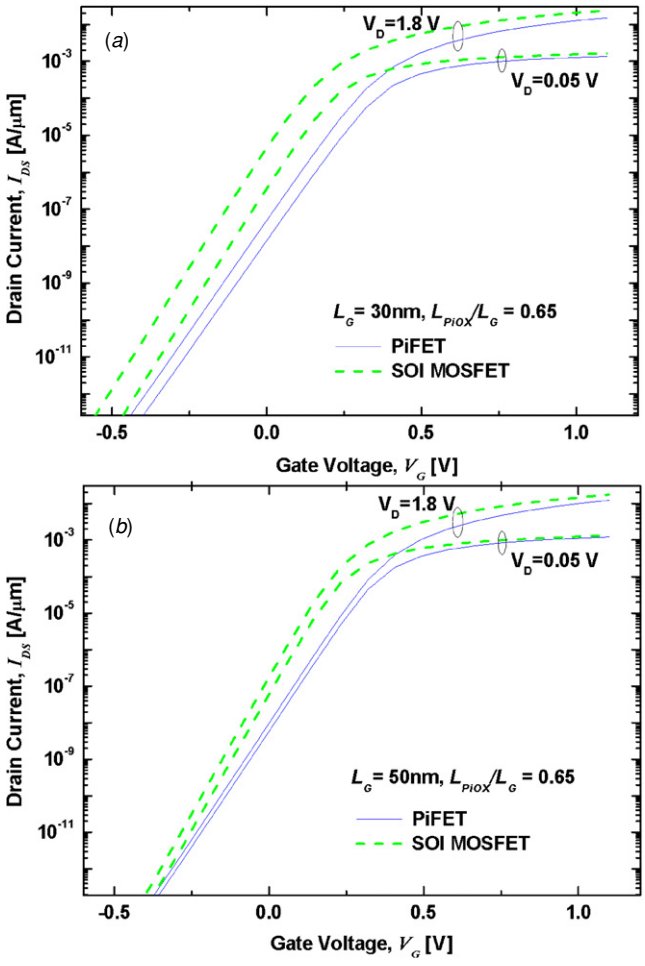

Figure 5. I_{DS}–V_g characteristic of the SOI MOSFET and PiFET (*a*) $L_g = 30$ nm (*b*) $L_g = 50$ nm.

the reduction effect is less significant than increasing T_{PiOX} as shown in figure 8.

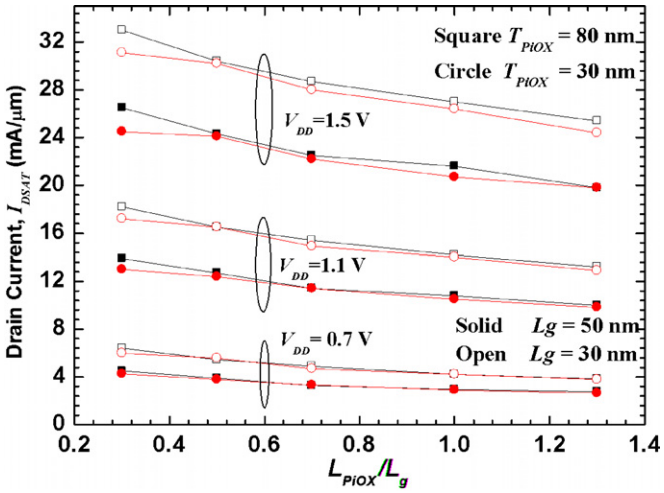

Figure 6. V_{DD} dependence of I_{DSAT} as a function of T_{PiOX} and L_g.

In addition, consequently, a thinner T_{PiOX} makes the circuit performance of PiFETs more layout and fanout dependent. It is shown that the large-size driver using the PiFET should be carefully designed because C_j in PiFETs is comparable to C_g. Nevertheless, trying to reduce C_j by making T_{PiOX} as large as possible induces a serious problems in both the fabrication process and the thermal conduction of self-heating. Actually, it is found that the decreased trend of C_j is saturated at $T_{\mathrm{PiOX}} \approx 60$ nm as shown in figure 9.

The L_g and V_{DD} dependence of the intrinsic gate delay, estimated from figures 6 and 7, is shown in figure 10. The intrinsic delay τ of a 30–50 nm long PiFET is lower than that of ITRS 32 nm technology node by more than 20%. Although the L_{PiOX}/L_g smaller than the SCE optimum value (=0.6–0.65) would further reduce C_j (eventually τ), the optimal conditions in perspective of both SCE and the circuit performance are $T_{\mathrm{PiOX}} \geqslant 60$ nm and $L_{\mathrm{PiOX}}/L_g = 0.6$–$0.65$, respectively, because

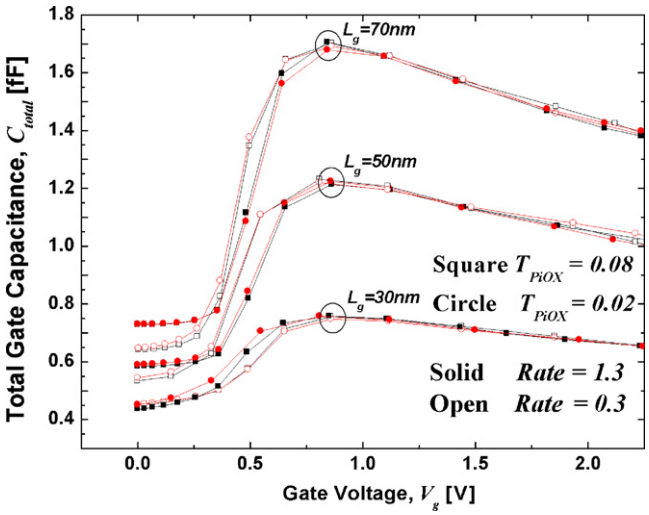

Figure 7. The C_{total}–V_g curve as a function of T_{PiOX}, L_{PiOX}/L_g and L_g.

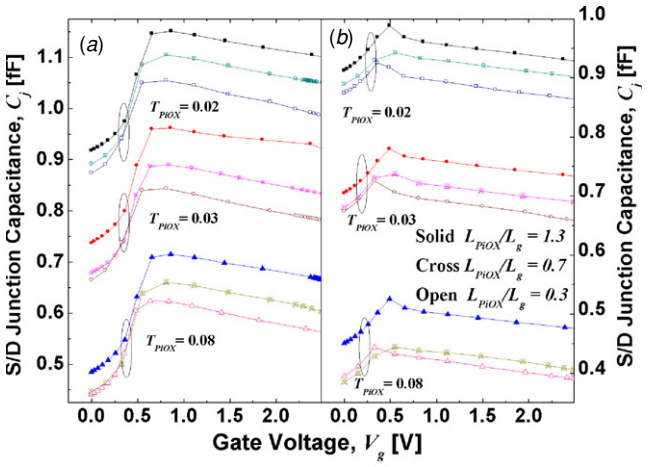

Figure 8. C_j–V_g curves extracted from the TCAD simulation as a function of L_{PiOX}/L_g, T_{PiOX} and L_g. (*a*) $L_g = 50$ nm and (*b*) $L_g = 30$ nm.

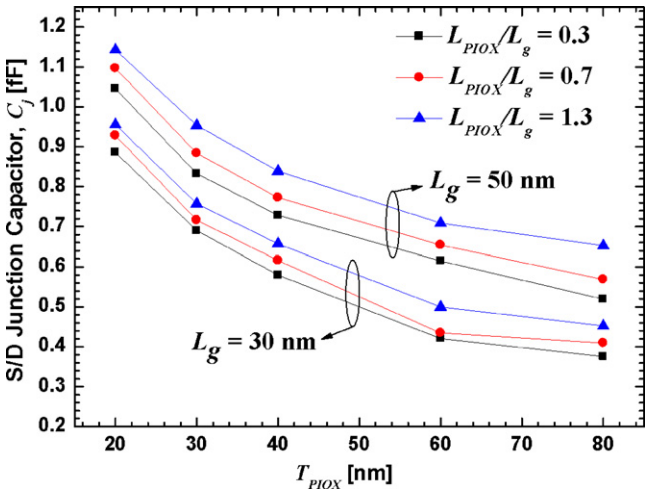

Figure 9. T_{PiOX} dependence of C_j as a function of L_{PiOX}/L_g and L_g.

C_j is the weak function of L_{PiOX}/L_g (compared with the extent of the T_{PiOX} dependence).

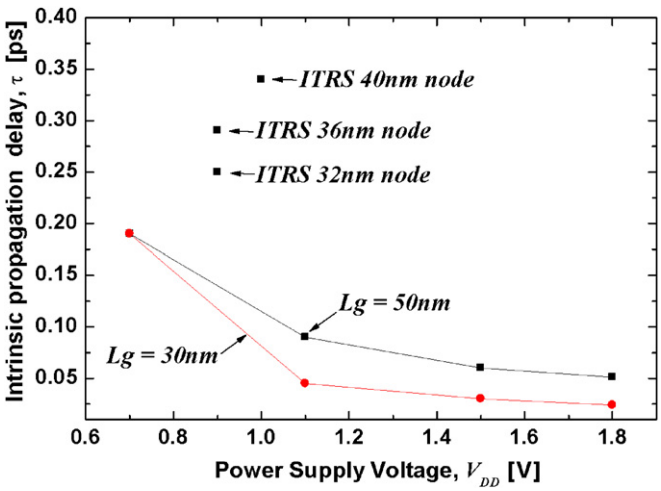

Figure 10. L_g and V_{DD} dependence of the intrinsic delay τ.

5. Conclusion

The L_{PiOX} and T_{PiOX} dependences of both SCE and the intrinsic delay in PiFETs have been investigated by using a TCAD device simulation. The RSCE can be suppressed by controlling the tilt angle of halo implantation at $T_{\text{tilt}} = 55^\circ$. As L_{PiOX}/L_g decreases, SSW becomes smaller while DIBL gets larger. The L_{PiOX}/L_g and T_{PiOX} dependence of the intrinsic delay results from the variation of junction capacitance C_j. The C_j is more sensitive to T_{PiOX} rather than L_{PiOX}/L_g. Smaller T_{PiOX} makes the circuit performance of PiFETs more layout- and fanout dependent. Conclusive optimal conditions for both SCE and the intrinsic delay are summarized as $L_{\text{PiOX}}/L_g = 0.6$–$0.65$, $T_{\text{PiOX}} \geqslant 60$ nm and $T_{\text{tilt}} = 55^\circ$. Our result shows that all of L_{PiOX}, T_{PiOX} and T_{tilt} are critical parameters controlling all of SSW, DIBL, RSCE and circuit performance in PiFETs.

Acknowledgments

This work was supported by the National Research Foundation (formerly KOSEF) grant funded by the Korean government (MEST) (no R01-2007-000-20879-0) Korea and the CAD software was supported by the IC Design Education Center (IDEC).

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