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Low Power/High Speed Compact ADCs based on SET(Single-Electron Transistor)/CMOS Hybrid Circuits

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Abstract

Two-types of SET (Single-Electron Transistor)/CMOS hybrid analog-to-digital converters (ADCs) for ultra-low power and high performance applications are proposed. In comparison with conventional CMOS flash-type ADCs, while the former shows the intrinsic conversion rate of about 20 % and the lower operating power by two orders of magnitude, the latter shows slightly higher conversion rate and the lower operating power by one order. In addition, the number of required transistors in SET/CMOS hybrid ADC is about 10-20 % of that in CMOS flash-type ADCs. Used SET model fully accounts for non-ideal effects in practical Si-based SETs and the peak-to-valley current ratio of SET has the range of 1.15~1.5. This is consistent with the experimental result of top-down approached Si-based SETs at 77~100 K.

I. Introduction

Analog-to-digital converters (ADCs) are crucial core blocks in modern signal processing systems with higher integration density, faster conversion speed, and lower power. In order to challenge to these requirements, Si single-electron transistor (SET)-based ADCs have been proposed having potential advantages of high integration density, ultra-low power dissipation, and extremely simple structure [1-4]. Although previous studies provide us a good guide for the design and optimization of SET-based ADC circuits in a real VLSI chip, there are two viewpoints to be considered. One is that models used in the circuit demonstration (*e.g.* Monte Carlo model) do not fully account fo practical non-ideal effects such as the control gate bias (V_{cg})-dependence of the tunneling resistance, parasitic field-effect transistor(FET) operation, and phase shift of Coulomb oscillation by the gate bias other than the main control gate which have been commonly observed in demonstrated Si-based SETs [5-11]. The other is that not transient but only DC characteristics of SET and/or SET/CMOS hybrid ADCs have been reported [1-4]. It is found in literatures that the time scale of transient characteristics has such an arbitrary unit that the speed of ADC response cannot be quantitatively estimated. It is mainly due to the weakness of SETs with a low current drivability.

In perspective of this, complementary SET/CMOS hybrid amplifier-based ADC has been already proposed in the previous work [12]. It was implemented with physics-based SPICE model including non-ideal effects. Moreover, the transient operation of SET/CMOS hybrid circuit-based ADCs fully accounting for non-ideal effects of real SETs was successfully demonstrated for the first time.

In this work, we propose SET/CMOS hybrid ADCs for two applications, *i.e.* ultra-low power (*ULP*) and high performance (*HP*). Furthermore, their performance parameters are compared with those of CMOS flash-type ADCs. Used SET model (Lee's SPICE model) fully accounts for non-ideal effects in real Si-based SETs and is well matched with experimental results over the wide range of a temperature and bias [13]. The peak-to-valley current ratio (PVCR) of SET has the range of 1.15~1.5 with V_{cg} of 0~6 V. Compared with the previous SET-based ADCs, our ADC makes features of the immunity to non-ideal effects, large voltage swing of the output signal, and high load drivability.

II. Simulation Results and Discussions

The equivalent circuit diagram of SET with depletion gates is shown in Fig. 1. SETs with depletion gates are generally known to be most promising solutions for SET/CMOS hybrid circuits in terms of their compatibility with extremely scaled CMOS VLSI technology, controllability, and reproducibility [14]. C_{cg} is the capacitance between the Si island and the control gate, and C_{sg} is the capacitance between the Si island and the depletion gate. Fig. 2 shows the architecture of a 4-bit SET/CMOS hybrid ADC. It comprises of a sample and hold block, a capacitive divider, and repeated core blocks. First main difference between CMOS ADCs and proposed SET/CMOS hybrid ADCs is that while a sampled input V_{in} is compared with pre-coded reference V_{ref} in the former, it is divided and self-generated-coded in the latter. Second is that while the latter requires only 4 SET/CMOS hybrid circuit blocks for a 4-bit conversion with an aid of the periodic nature of SET current, both the thermometer code and 2^4–1 comparators are required in the former. Therefore, the density of SET/CMOS hybrid ADCs can be dramatically increased in comparison with CMOS ADCs.

Fig. 3 shows the core block of the proposed *ULP* SET/CMOS hybrid ADC. Its operation scheme is the combination of both the amplification of SET current by FET and the suppression of a Coulomb blockade oscillation valley current by the differential amplification. Furthermore, the full V_{dd} swing of an output signal is obtained in comparison with only SET-based ADCs. Here, the PVCR of SET has the range of 1.15~1.5 with V_{cg} of 0~6 V, which is consistent with the experimental result of top-down approached Si-based SETs at 77~100 K. The load drivability is also considerably higher than the case of SET-based ADCs although the operation speed is still limited by the drivability of SET. The 4-bit conversion rate is 22 MHz at V_{dd}=1.2 V with V_{in}=0~6 V. Here, the conversion rate is defined in terms of the ramped V_{in}, and the rate of a sample and hold block is ruled out in order to estimate the intrinsic conversion speed. Fig. 4 shows the core block of proposed *HP* SET/CMOS hybrid ADCs. By adding two stages of the differential amplifiers, both the input signal swing and the conversion speed are improved. Fig. 5 shows the transient characteristic of a 4-bit *HP* SET/CMOS hybrid ADC. The 4-bit conversion rate is 111 MHz at V_{dd}=1.2 V, V_{in}=0~6 V.

In order to benchmark the performance of proposed ADCs, a conventional CMOS flash-type ADC based on standard 0.18-μm CMOS technology ($V_{TN}=|V_{TP}|=0.5$ V) is also implemented and its performance is estimated by HSPICE simulation. Fig. 6 shows the circuit diagram of a comparator used in flash-type CMOS ADCs. The 4-bit conversion rate is 105 MHz at V_{dd}=1.2 V and V_{in}=0~1.2 V. Fig. 7 shows the INL/DNL characteristics of respective 4-bit ADCs. They are within the range of –0.5~0.5 LSBs. Finally, the result of benchmarking performance parameters are summarized in Table. I. It is noticeable that *HP* SET/CMOS hybrid ADC shows an intrinsic conversion rate slightly higher than that of the CMOS flash-type ADC even in the wider range of input signal. We also note that *ULP* SET/CMOS hybrid ADC shows an operating power lower by two orders of magnitude than that of CMOS flash-type ADC. In addition, the number of required transistors in SET/CMOS hybrid ADC is about 10-20 % of that in CMOS flash-type ADC.

III. Conclusions

SET/CMOS hybrid ADCs for two applications (*ULP* and *HP*) are proposed and their performances are successfully demonstrated. Our result shows the trade-off between the intrinsic conversion rate and the power consumption. While the *ULP* SET/CMOS hybrid ADC shows an operating power lower by two orders of magnitude than that of CMOS flash-type ADC, the number of required transistors is about 10 % of that in CMOS flash-type ADC. Used SET model (Lee's SPICE model) fully accounts for non-ideal

effects in practical Si-based SETs and the PVCR of SET has the range of 1.15~1.5. It manifests the feasibility of a robust design of ultra-power-efficient SET/CMOS hybrid ADCs.

Acknowledgements

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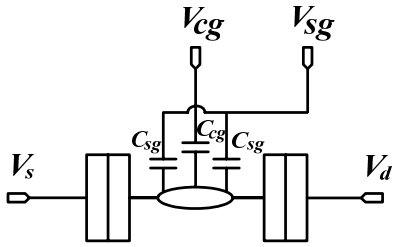

Fig. 1. The schematic of circuit diagram of Si-based SET with depletion gate.

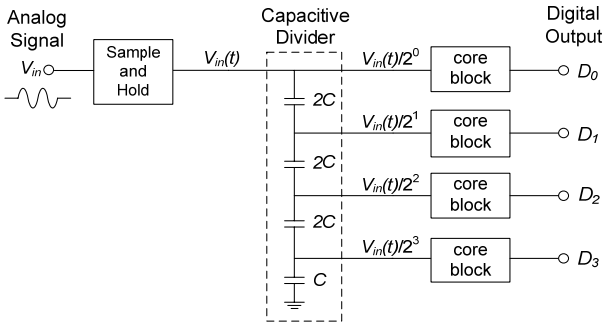

Fig. 2. Architecture of 4-bit SET/CMOS hybrid ADCs.

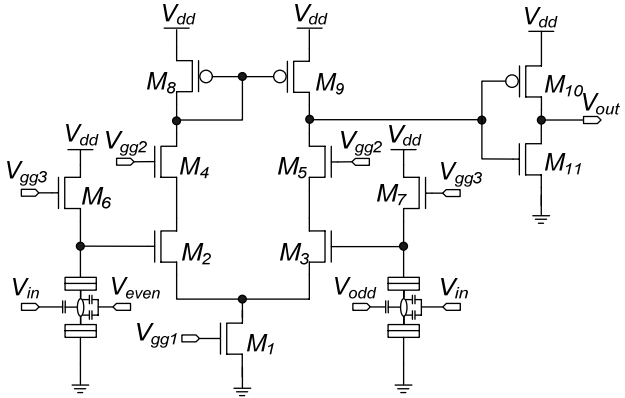

Fig. 3. Schematic circuit diagram of the core block of *ULP* SET/CMOS hybrid ADCs. V_{dd}=1.2 V, V_{odd}=0.16 V, V_{even}=0 V, V_{gg1}= -0.1 V, V_{gg2}=0.1 V, V_{gg3}= -0.3 V. The SET device parameters: C_{cg}=0.24 aF, C_s=C_d=1.3 aF, R_s=R_d=1.3 MΩ (Corresponding to the Si island size of 40×30 nm^2). MOSFET parameters: *W*/*L*=10/0.5 μm for nMOSFET (M1), *W*/*L*=10/0.18 μm for nMOSFET (M2 and M3) as a current amplifier, *W*/*L*=10/0.5 μm for nMOSFET (M4 and M5), *W*/*L*=2/0.18 μm for nMOSFET (M6 and M7) as a buffer, *W*/*L*=10/0.5 μm for pMOSFET (M8 and M9) as a current mirror, *W*/*L*=2/0.18 μm for pMOSFET (M10) and *W*/*L*=1/0.18 μm for nMOSFET (M11) as a inverter, respectively.

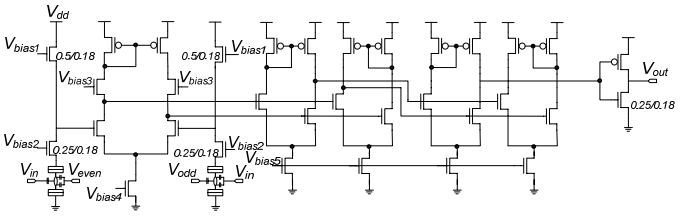

Fig. 4. Schematic circuit diagram of the core block of *HP* SET/CMOS hybrid ADCs. V_{dd}=1.2 V, V_{odd}=0.16 V, V_{even}=0 V, V_{biasp}= -0.1 V, V_{gg2}=0.1 V, V_{gg3}= -0.3 V. The SET device parameters: C_{cg}=0.24 aF, C_s=C_d=1.3 aF, R_s=R_d=1.3 MΩ. MOSFET parameters: *W*/*L*=2.5/0.18 μm for unlabeled pMOSFETs and *W*/*L*= 1/0.18 μm for unlabeled nMOSFETs.

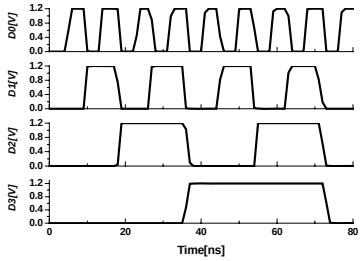

Fig. 5. Simulated transient conversion characteristic of a 4-bit *HP* SET/CMOS hybrid ADC

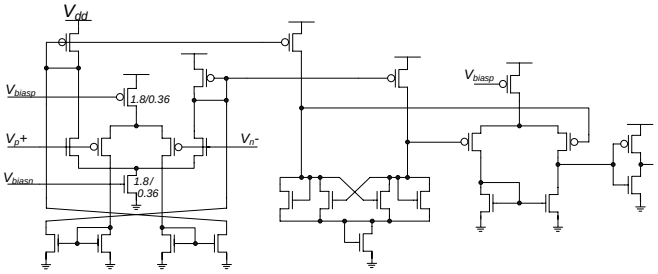

Fig. 6. Schematic diagram of the comparator in CMOS flash-type ADCs with rail-to-rail input common-mode range. V_{dd}=1.2 V, V_{biasp}=0.6 V, V_{biasn}=0.5 V. MOSFET parameters: *W*/*L*=3.6/0.18 μm for unlabeled pMOSFETs and *W*/*L*= 1.8/0.18 μm for unlabeled nMOSFETs.

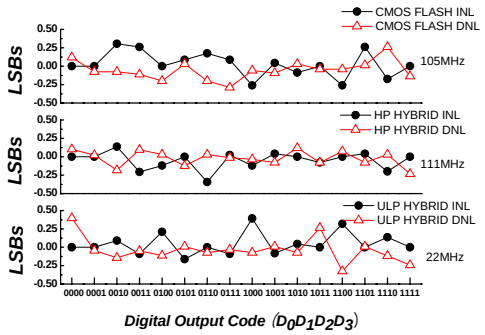

Fig.7. INL and DNL characteristic of a 4-bit *HP* SET/CMOS hybrid ADC.

Table I. Comparison of performance parameters between SET/CMOS hybrid ADCs and CMOS flash-type ADCs

ADC type / Parameters	*ULP* SET/CMOS hybrid	*HP* SET/CMOS hybrid	CMOS Flash-type
V_{dd}	1.2 V	1.2 V	1.2 V
Input range	0~6 V	0~6 V	0~1.2 V
Conversion rate	22 MHz	111 MHz	105 MHz
Temperature	77K(SET) & R.T (CMOS)	77K(SET) & R.T (CMOS)	R.T
Operating power (W)	2.2e-05	5.7e-04	2.4e-03
Standby power (W)	5.9e-11	8.8e-10	7.4e-07
No. of Transistors	44	140	465