P-203L: *Late-News Poster:* Analysis on AC Stress-Induced Degradation Mechanism of Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistor Inverters

Sungchul Kim, Yong Woo Jeon, Sangwon Lee, Dong Myong Kim, and Dae Hwan Kim [a]

School of Electrical Engineering, Kookmin University, Jeongneung-dong, Seongbuk-gu, Seoul 136-702, Republic of Korea.

Sang Wook Kim, Sun Il Kim, Jaechul Park, U-In Chung, and Chang-Jung Kim

Samsung Advanced Institute of Technology (SAIT), San #14-1, Nongseo-Dong, Yongin 446-712, Republic of Korea.

Abstract

The degradation mechanism of a-IGZO TFT-based inverter is investigated under the toggled AC biased input (V_{IN}), with a direct evidence of subgap density of states (DOS). The AC stress-induced threshold voltage shift (ΔV_T) of driver TFT is observed to be smaller than that of load TFT, which results in the V_{OH} degradation during AC stress. The dominant mechanism of the toggled V_{IN} stress-induced ΔV_T of driver TFT in a-IGZO inverter is the increase of subgap DOS deep stats, whereas the ΔV_T of load TFT during inverter operation is attributed to the electron trapping into the interface and/or a-IGZO thin film.

1. Introduction

The focus of recent works on amorphous oxide semiconductor (AOS) thin film transistors (TFTs) has been fast transferred from fundamentals in perspective of material science and engineering to reliability studies in viewpoint of their application-dependent manufacturabilities. As in-depth understanding of the electrical characteristics in AOS TFTs based on material science and process technology becomes more mature, the underlying mechanism on the electrical stress/temperature/optical illumination/layout-dependent degradation and/or instability under a real circuit operation condition has been more and more significant issue. For examples, the driving current-induced threshold voltage (V_T) shift (ΔV_T) should be considered for active-matrix organic light-emitting diode (AMOED) driver TFTs applications [1, 2]. In terms of the switch TFTs in large-area high-resolution active-matrix liquid crystal display (AMLCD) backplanes [3, 4] and/or AMOLED, the negative bias-induced ΔV_T under ambient light from backlight unit has to be most importantly analyzed because their bias condition lies in OFF state during most of each cycle time. In addition, the toggled AC bias stress-induced degradation would be emerged as a critical reliability issue of AOS TFT-based logic circuit such as the decoder in 3-D stack memories [5, 6]. However, up to now, the reliability issues such as a constant current/positive bias/negative bias/temperature stress-induced ΔV_T and an optical sensitivity have been investigated not under a real circuit operation condition but in a single TFT level [7-12], so that a dynamic bias condition has been unable to be reflected. It should be noted that the accurate projection and elucidation of diverse reliability issues **only in real circuit operations** play a significant role of assessing the feasibility of various innovative AOS TFT-based applications. Motivated by these backgrounds, in this work, the degradation mechanism of amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) TFT-based inverter, as a representative AOS TFT, is investigated under a real logic operation condition (*i.e.*, toggled AC biased input). For the first time, the respective AC bias time-evolution of subgap density of states (DOS) in the load and driver TFTs in the case of enhancement load-type a-IGZO inverter is characterized and discussed.

2. Experiments

The brief procedure of the a-IGZO TFT fabrication is as follows: On a thermally grown SiO_2/Si substrate, the first sputtered deposition at room temperature (RT) and patterning of molybdenum (Mo) gate are followed by PECVD deposition of gate dielectric SiO_2 at 300 ^oC. A a-IGZO active layer (In_2O_3:Ga_2O_3:ZnO= 2:2:1 at %) is then sputtered by the RF magnetron sputtering at RT in a mixed atmosphere of Ar/O_2 (100:1 at sccm) and patterned by wet etch process with diluted HF. For the formation of source/drain (S/D) electrodes, Mo is sputtered at RT and then patterned by dry-etching. After N_2O plasma treatment on the channel surface of a-IGZO active layer, a SiO_2 passivation layer is continuous deposited at 150 ^oC by PECVD without a vacuum break. Finally, the anneal in the furnace at 250 ^oC is performed for 1 hr.

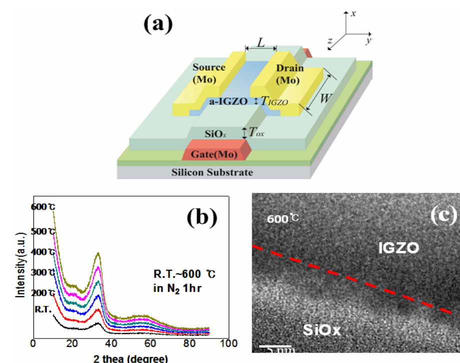

Fig. 1. (a) Schematics of integrated a-IGZO TFT, (b) XRD and (c) TEM view of the fabricated a-IGZO layer.

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[a] electronic mail:drlife@kookmin.ac.kr