A Novel Superlattice Band-gap Engineered (SBE) Capacitorless DRAM Cell with Extremely Short Channel Length Down to 30 nm

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Abstract

We propose a novel SiGe superlattice band-gap engineered (SBE) capacitorless dynamic random access memory (DRAM) cell with the 30 nm channel by the 2D TCAD simulation. The SBE capacitorless DRAM cell used a common source structure and different metal layers for the top gate word line from the bottom gate word line to realize the $4F^2$ ($0.0036\ \mu m^2$) feature size. From the 2D TCAD simulation of the SBE capacitorless DRAM cell, thanks to both the $Si_{0.8}Ge_{0.2}$ quantum well and SiO_2 physical energy barrier, we obtained the sensing margin of 6.4 μA and the retention time of 15 msec.

I. Introduction : Why a New DRAM Cell ?

Up to date, capacitorless DRAM cells are under active study to overcome the scaling limit of the conventional capacitorless/1T DRAM cell. In order to solve these problems in reported capacitorless DRAMs, many researchers employed $Si/Si_{1-x}\ Ge_x$ heterostructures to utilize the band offset in the valence band (quantum well for hole confinement). It has been a long time that Si/SiGe heterostructures are utilized in a HBT because it offers a large energy barrier against back injection of carriers from the base, high carrier mobility, and high cutoff frequency. However, one of the obstacles to the production of defect-free SiGe epitaxy layers is the generation of dislocations caused by the strain relaxation at the substrate/epitaxy layer interface. Threading dislocations formed in the SiGe layer degrade the material quality resulting in poor device performance (lifetime, mobility and recombination current) due to interface states [1-2]. Several authors have proposed a variety of methods to reduce the number of threading dislocations, including superlattice and step-graded layers [3-4]. Here, we should consider the generation of dislocations caused by the strain relaxation in order to adopt Si/SiGe heterostructures in capacitorless DRAM applications.

Many researches employing Si/SiGe heterostructures for the capacitorless DRAM cell used a thick SiGe layer with high Ge mole fraction to get a large bandgap discontinuity at the Si/SiGe heterojunction. In those cases, the energy band offset is not consistent with what they expected because of the strain energy relaxation. In addition, a single SiGe layer with high Ge mole fraction causes high density of defects and finally obtains poor electrical performance including the excess carrier lifetime which is related to the retention of the charge storage .

In this work, a Novel Capacitorless DRAM Cell employing a thin $Si_{0.8}Ge_{0.2}$ storage layer with a band-gap engineered Si/SiGe heterostructure superlattice layers and SiO_2 energy barrier is proposed to resolve such critical issues. Moreover, a SiO_2 physical energy barrier structure is introduced to prevent generated holes from being swept out during the impact ionization as well as to improve the retention characteristic.

II. Proposal of a Novel Superlattice Band-gap Engineered (SBE) Capacitorless DRAM

The proposed Superlattice Band-gap Engineered (SBE) capacitorless DRAM cell is shown in Fig. 1(a). The SBE capacitorless DRAM cell has a crystallized Si channel and a strained $Si_{0.8}Ge_{0.2}$ storage layer under the Si channel. Since the band-gap of the strained SiGe storage layer is smaller than that of the Si (~1.12 eV) layer, there is a band offset between the SiGe layer and the Si layer as shown in Fig. 1(b). In this case, because the SiGe layer is grown on a relaxed Si layer with 20 % of Ge, almost the entire band offset occurs in the valence band (0.14 eV) while the band offset in the conduction band (0.036 eV) is very small. The thickness of the SiGe storage layer is decided in the range of the *critical thickness* to keep a strained state without inducing crystal defects [5]. The repeated Si/SiGe epitaxial layers under the SiGe storage layer are grown up to reduce defects from Si/SiGe lattice mismatch.

The SBE capacitorless DRAM cell structure is

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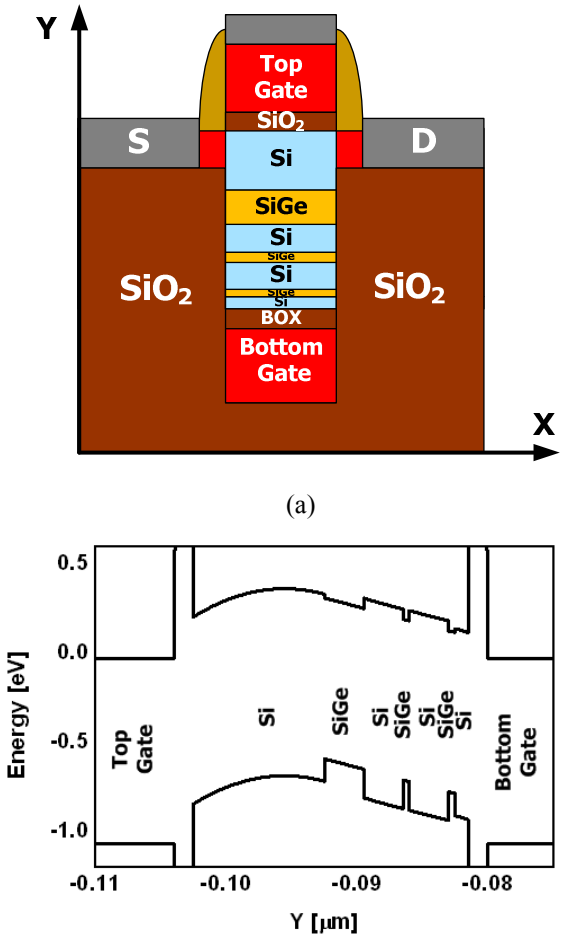
distinguished by the Silicon-oxide (SiO_2) physical barrier. Without the SiO_2 physical barrier, the SBE capacitorless DRAM cell cannot accumulate holes generated by the impact ionization to write data '1' even if it employs the SiGe layer on the Superlattice structure. This is because the generated holes are swept out to the source in the 30 nm channel length.

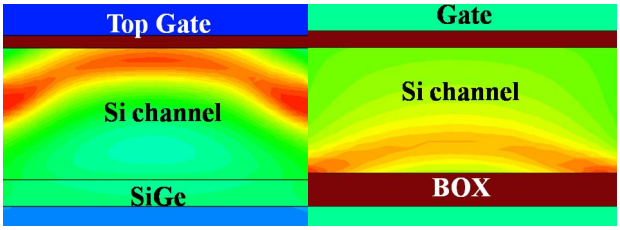


(a)

(b)

Fig. 1 (a) A cross-sectional view of the proposed Superlattice Band-gap Engineered (SBE) capacitorless DRAM cell structure and (b) the energy band diagram for the top gate to the bottom gate through the SBE layer

Moreover, since the Shockley-Read-Hall (SRH) recombination rate increases in proportion to the product of electron and hole concentration, conventional SOI capacitorless DRAM cells have a high SRH recombination rate. As a result, it leads to a high leakage current and cannot retain holes for the data storage. However, the SiGe storage layer of the proposed SBE capacitorless DRAM cell structure does not reach to the n^+ S/D region. Therefore, the retention time would be significantly improved. Fig. 2 comparatively shows the SRH recombination rate of (a) the SBE capacitorless DRAM cell and (b) a conventional SOI planar capacitorless DRAM cell. In the case of the SBE capacitorless DRAM cell, most of the SRH recombination occurs in the channel region not in the SiGe storage layer. On the contrary, the conventional SOI planar capacitorless DRAM cell shows that a larger SRH recombination occurs in the floating body region. In addition, the SBE capacitorless DRAM cell has a shallow body-to-S/D junction and it allows a reduction of the parasitic bit line capacitance up to 38 %. Employing a metal-silicide process, parasitic resistances in the source/drain region can be further improved.



(a) (b)

Fig. 2 (a) A conventional SOI planar capacitorless DRAM cell (channel length=100 nm) shows high SRH recombination rate (~$1x10^{23}$ $cm^{-3}s^{-1}$) in the storage region whereas (b)Relatively low SRH recombination (~$3x10^{22}$ $cm^{-3}s^{-1}$) occurs in the channel region of the SBE capacitorless DRAM cell (channel length=30 nm).

We considered a process flow for practical implementation during the 2D TCAD simulation and an expected process sequence is shown in Fig. 3. The SBE capacitorless DRAM can be established either on a bulk Silicon wafer or on an SOI wafer. And then the bottom gate is defined by the damascene process after ELO process [6]. When an SOI wafer is used, the bottom gate is defined just by damascene process without SiO_2 deposition (Fig. 3(a) ~ (c)). Note that the bottom gate should be wider than the channel width for the bottom gate contact. Details are provided at the end of this section with cell array schematics.

In the proposed process flow, we used 3 masks to define the bottom gate, the channel, and the top gate. Therefore, there is a possibility of being misaligned from each other. To achieve more robust verification, we also assessed the misalignment effects during practical implementation. In other words, we may expect that the process margin for the SBE capacitorless DRAM cell is 4 nm (13 %).

Fig. 4(a) shows a bird's view of the SBE capacitorless

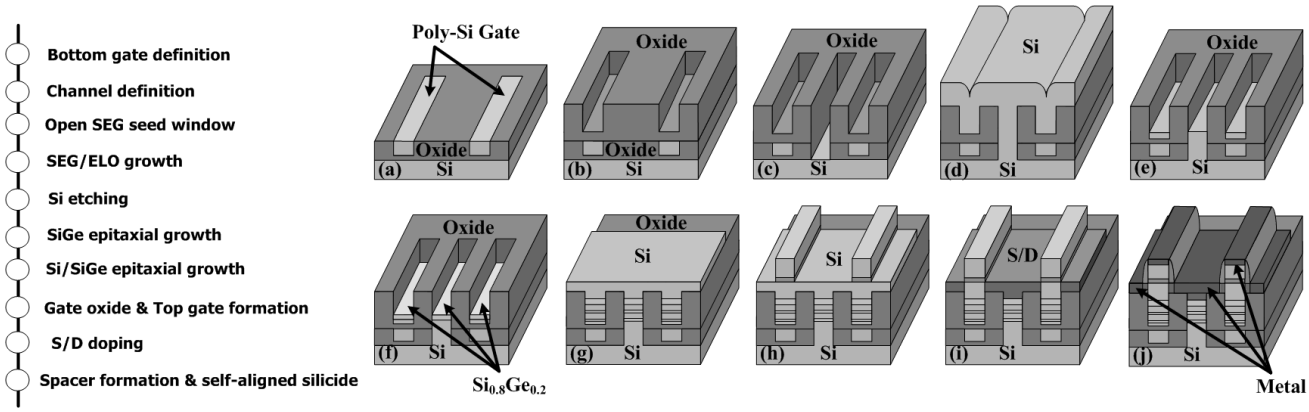


Fig. 3 Process flow of SBE Capacitorless DRAM cell

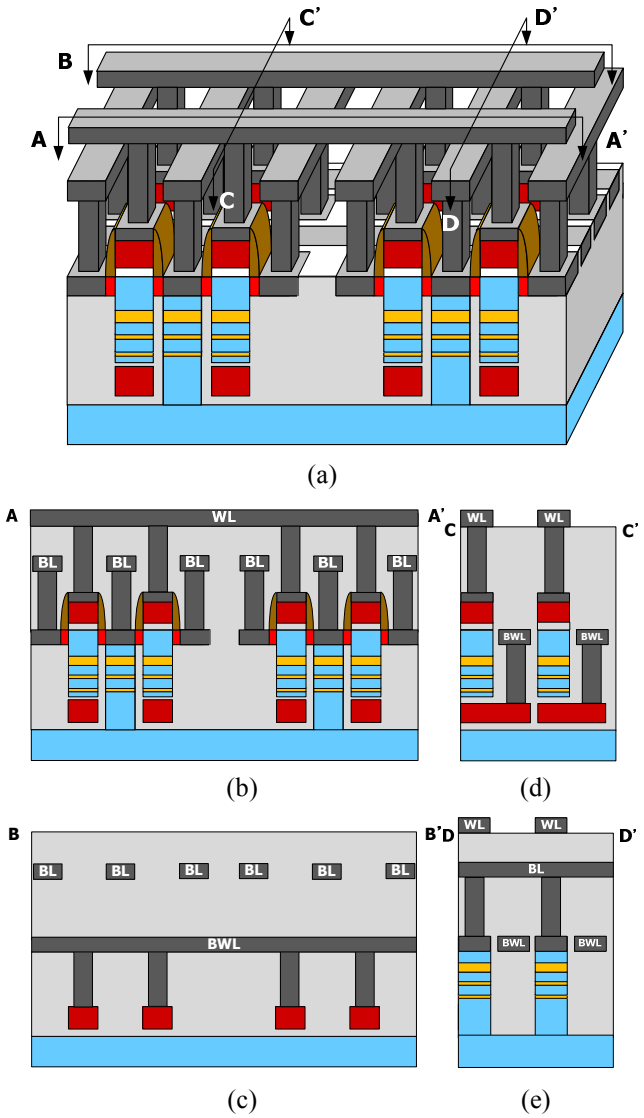


Fig. 4 (a) Bird's view of the proposed SBE capacitorless DRAM cell array (4 × 2) (b) A-A' and (c) B-B' cross section view along the length direction (d) cut view along C-C' and (e) cut view along the width direction (D-D') (c) the energy band diagram for the top gate to the bottom gate through the SBE layer

DRAM cell array. The proposed SBE capacitorless DRAM cell has two word lines (WLs). Here, if two WLs are on the same metal layer, its feature size cannot be small due to the word line pitch limit. In this work, to make a $4F^2$ feature size, the top gate word line (WL, metal 3) and the bottom gate word line (BWL, metal 1) use different metal layers from each other. BWL on the bottom is formed between two active regions so it seems like a buried word line. WL on the top is the same as in the conventional one. The SBE capacitorless DRAM cell is realized in the $4F^2$ ($0.0036\ \mu m^2$) feature size even though it employs two gate electrodes (or WLs).

III. Memory Characteristics

The sequence of the operation is as follows. First, to write data '1', both top gate and drain are biased at 1.2 V for 50 ns while the bottom gate is biased at 0.0 V. And then -1.2 V bias is applied to the bottom gate to keep holes. After 20 ns holding operation, 0.5 V is applied to the top gate with V_{DS}=0.3 V in order to read the stored data. The read condition can be modified to obtain a large current in the linear mode. The accumulated holes are swept out when both the top gate and the drain are biased at -1.2 V with the bottom gate biased at 1.2 V.

Transient characteristics of the source current are shown in Fig. 5. The TCAD 2D device simulation is performed with the 30 nm channel length and width, combining advanced physical models with quantum effects, tunneling mechanisms, and mobility models [7]. The conventional SOI planar structure is a conventional SOI capacitorless DRAM cell W/L= 30 nm/ 30 nm. The inset is a magnification of the source current to show the sensing margin between data '1' and '0'. As can be seen in the inset, The SBE capacitorless DRAM cell with W/L= 30 nm/ 30 nm has sensing margin of 6.4 μA. This is sufficient to be

sensed by the current sense amplifier. However the sensing margin of the conventional one is too small to determine the stored data.

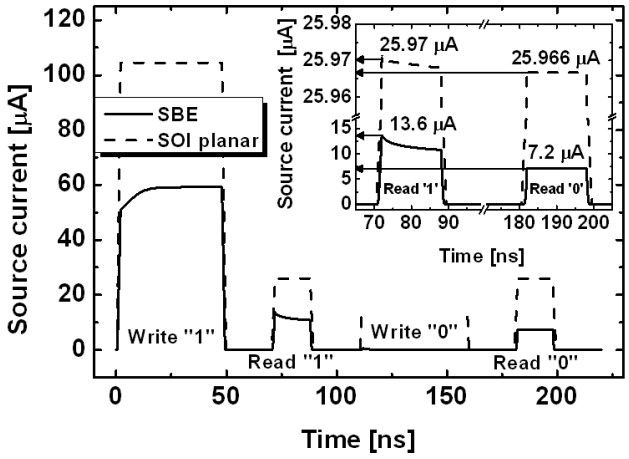


Fig. 5 Transient characteristics of the SBE capacitorless DRAM cell with W/L= 30 nm/ 30 nm, compared with a conventional SOI planar capacitorless DRAM cell with W/L= 30 nm/ 30 nm

The retention time is defined as the time it takes either for the source current of the '1' or '0' state to reach its steady state value when the hold time, following as write operation, increases. The steady state current is approximately the median value of the read '0 and read '1' current. Considering the sensing method of the capacitorless DRAM cell, such definition of the retention time is justifiable. Retention time can be obtained by measuring the source current while increasing the hold state time after the write operation.

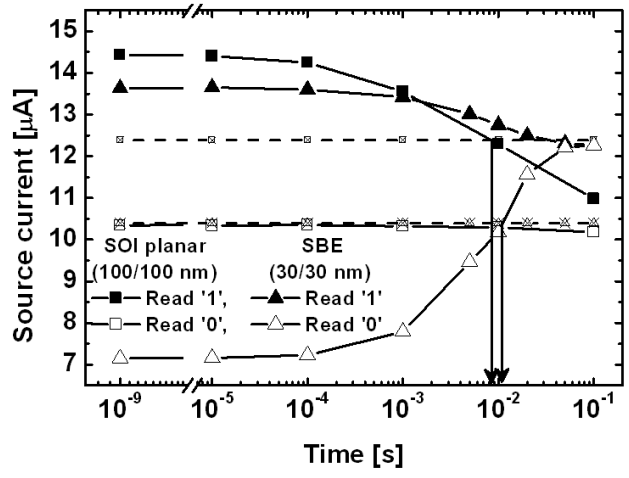


Fig. 6 Retention characteristics (The black square symbols for the W/L=100/ 100 nm SOI conventional capacitorless structure and the red circle symbols for the W/L=30/ 30 nm SBE structure)

The retention characteristics of the SBE capacitorless DRAM cell are shown in Fig. 6. To evaluate how well the retention time is improved, the conventional SOI planar capacitorless DRAM cell simulations were performed respectively. Fig. 3.6(a) shows the retention time of the SBE structure comparing with the W/L= 100 nm/ 100 nm SOI planar structure. (Because the W/L= 30 nm/ 30 nm conventional SOI planar capacitorless DRAM cell has very low sensing margin, we simulated the conventional SOI planar capacitorless DRAM cell with W/L= 100 nm/ 100 nm.) As we've expected, the ability to hold generated holes in the SOI planar structure is improved by the SBE structure.

V. Summary and Conclusion

In this work, the proposed a novel superlattice band-gap engineered capacitorless DRAM cell with a 30 nm channel length is expected to be a strong candidate for the solution. The storage layer with the $Si_{0.8}Ge_{0.2}$ band-gap engineered superlattice heterostructure under the Si channel improved the retention characteristic by the hole confinement which is advantageous from the band offset between the Si layer and SiGe layer. In addition, the physical barrier made of the SiO_2 layer prevented generated holes from being swept out during write data '1' operation and contributed to the reduction of the SRH recombination in the SiGe storage layer. As a result, we obtained the sensing margin of 6.4 μA and the retention time of 15 msec from the 2D TCAD simulation. For practical implementation, we considered the Si/SiGe superlattice structure as well as the critical thickness to reduce defects from the lattice mismatch and the misalignment effect. In order to reduce the cell feature size, the different metal layer was employed for the top gate word line from the bottom gate word line. As a result, $4F^2$ ($0.0036\ \mu m^2$) of the cell size was realized

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