[WD4-E-6]

Photoresist removal on GaAs surface using organic solvents

Eunseok Oh, Sehyun Oh, Junwoo Lee and Sangwoo Lim*

Department of Chemical and Biomolecular Engineering, Yonsei University, Seoul 03722, South Korea

(E-mail : swlim@yonsei.ac.kr)

현재 실리콘 기반의 트랜지스터는 높은 작동전압, 누설 전류 등의 문제로 집적도 향상이 물리적 한계에 도달하였다. 반면 III-V 족 화합물 반도체는 실리콘에 비하여 높은 전자 이동도를 가지고 있어 소자의 power consumption 증가 등의 문제를 해결할 수 있다. 그러나, 이러한 III-V 족 화합물 반도체를 트랜지스터 제조 공정에 적용하기 위해서는 아직 해결해야 할 문제점들이 산적해 있다. 문제점들 중 한가지는 III-V 족 반도체 상의 포토레지스트 제거이다. 일반적으로 실리콘 상의 포토레지스트 제거에 사용되는 고온의 SPM과 오존수는 III-V 족 반도체 표면의 식각이나 산화를 발생시켜 적용하기 어렵다. 따라서, 본 연구에서는 GaAs 상의 이온 임플란트된 포토레지스트를 두 가지 서로 다른 특성을 갖는 유기용매에 연속적으로 담지하여 제거하였다. 첫 번째 단계에서는 상대적으로 낮은 몰부피를 갖는 유기용매인 formamide, acetonitrile, nitromethane, monoethanolamine 중 한가지에 담지하였으며, 두 번째 단계에서는 포토레지스트와 높은 친화도를 갖는 유기용매인 DMSO를 사용하여 GaAs 상의 임플란트된 포토레지스트를 제거하였다. 포토레지스트 제거 효과는 FE-SEM과 optical microscope를 이용하여 확인하였으며 XPS와 AFM을 통하여 GaAs의 표면상태의 변화를 분석하였다. 연구 결과, acetonitrile과 DMSO를 사용하였을 때 가장 효과적으로 이온 임플란트된 포토레지스트를 제거할 수 있었으며 두 용매는 GaAs 표면의 변형을 야기하지 않았다 (Fig. 1). 또한, 적절한 첨가물을 이용하여 trench 구조의 구석에 남는 포토레지스트의 residue까지 완벽히 제거할 수 있었다.

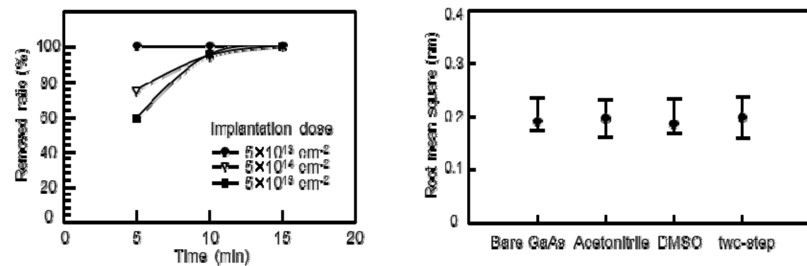

Figure 1. Acetonitrile + DMSO two-step sequence의 담지 시간에 따른 포토레지스트 제거율 (left), 유기용매 처리 전, 후 GaAs의 roughness (right)

[WD4-E-7]

High-performance $In_{0.53}Ga_{0.47}As$-OI MOSFET on Si substrates

Seong Kwang Kim[1,2], Jae-Phil Shim[1], Dae-Myeong Geum[1,3], Chang Zoo Kim[4], Han-Sung Kim[1], Yeon-Su Kim[1], Hang-Kyu Kang[1], Jin-Dong Song[1], Sung-Jin Choi[2], Dae Hwan Kim[2], Won Jun Choi[1], Hyung-jun Kim[1], Dong Myong Kim[2*] and SangHyeon Kim[1*]

[1]*Korea Institute of Science and Technology, Korea*, [2]*School of Electrical Engineering, Kookmin University, Korea*
[3]*Department of Materials Science and Engineering, Seoul National University, Korea*, [4]*Korea Advanced Nano Fab Center, Korea*

(E-mail : sh-kim@kist.re.kr, dmkim@kookmin.ac.kr)

InGaAs is the most preferred candidates for replacing silicon-based logic devices due to its high electron mobility and injection velocity [1]. Moreover, extremely-thin body and InGaAs-on-insulator (InGaAs-OI) structure are strongly needed to achieve both of good short channel effect control and high on state performance [2]. Here, in this study, we demonstrated high-performance top gate InGaAs-OI MOSFET using InGaAs-OI wafers fabricated by the direct wafer bonding (DWB) and epitaxial lift off (ELO) technique. The DWB accomplished by the ELO seems to be a very promising approach for high-quality III-V-OI/Si as well as a low cost process by re-use of the donor wafer.
For the device fabrication, we used n^+InGaAs/InP(cap)/InGaAs(intrinsic)/Y_2O_3(DWB)/Si substrate. Figure 1 shows the schematic image of final device structure. First, a mesa was defined by wet etching. Then, source and drain metal was deposited by electron beam (E-beam) evaporation, followed by gate recess etching. The n^+InGaAs was etched by citric acid and then InP was etched by digital etching process. Next, 10 nm-thick Y_2O_3 was depositied by E-beam evaporation. Then, 5 nm-thick Al_2O_3 was subsequently deposited by atomic layer deposition. Than, gate metal was deposited by E-beam evaporation. We obtained a good transfer curves with 10^6 on/off ratio and subthreshold swing of about 120 mV/dec as shown in Fig. 2. Also, the high peak mobility of approximately 2,800 $cm^2/V{\cdot}s$ was obatained as shown in Fig. 3, which is record-high among the reported surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs (Fig. 4).

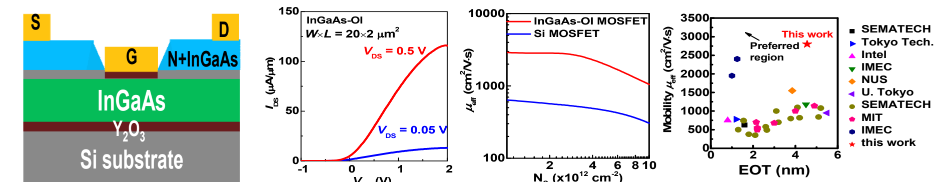

Fig. 1. Schematic image of InGaAs-OI MOSFET (**left**).
Fig. 2, 3. The transfer (**center-left**) and μ_{eff} (center-**right**) curves of InGaAs-OI MOSFET. Fig. 4. Benchmarks of μ_{eff} values with other reported surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs (**right**).

Reference

[1] J. A. del Alamo *et al.*, *Nature* **479**, p. 317 (2011), [2] S. H. Kim *et al.*, *APL* **105**, 043504 (2014)

Acknowledgment
This work was supported in part by KIST flagship program (2E26420), the future Semiconductor Device Technology Development Program (10052962), the National Research Foundation of Korea (NRF) grant (MEST) (2015004870), and the MSIP (2016R1A5A1012966) funded by the Korean government and in part by IC Design Education Center (IDEC).